10/807903

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: William D. Llewellyn

Attorney Docket No.: TRIPP040

Patent: 7,026,866 B2

Issued: April 11, 2006

Title: DC OFFSET SELF-CALIBRATION SYSTEM FOR A SWITCHING AMPLIFIER

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on September 21, 2006 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

CLAIMS:

1. In line 7 of claim 20 (column 10, line 15) change "byte" to --by the--. This appears correctly in Amendment A as filed on November 9, 2005,on page 5, claim 21, line 5.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. TRIPP040).

Respectfully submitted,
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19. (Original) An integrated circuit comprising the offset cancellation logic of claim 1.

20. (Original) An electronic system comprising the integrated circuit of claim 19.

21. (Currently amended) A switching amplifier comprising

a power output stage comprising first and second outputs forming a differential output, and first and second supply rails; and

a processor stage operable to receive an input signal and generate a processed differential signal for amplification by the power output stage, the processor stage further comprising offset cancellation logic which is operable in a calibration mode to generate a first offset cancellation signal when the first and second outputs are coupled to a first voltage corresponding to the first supply rail, and a second offset cancellation signal when the first and second outputs are coupled to a second voltage corresponding to the second supply rail, the offset cancellation logic further being operable to facilitate at least partial cancellation of an offset voltage associated with the different output during a normal operation mode using a third offset cancellation signal which substantially corresponds to an average of the first and second offset cancellation signals, wherein the offset cancellation logic comprises a digital-to-analog converter (DAC), a first up/down counter, a second up/down counter, and calibration control logic, the calibration control logic being operable to configure the amplifier for the calibration and normal operation modes, the calibration control logic further being operable during the calibration mode to control the first and second counters and the DAC via one of the counters to generate the first and second offset cancellation signals, the DAC being operable during normal operation mode to generate the third offset cancellation signal.

PTO/SB/44 (10-96)
Approved for use through 6/30/99. OMB 0651-0033
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

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DATED : April 11, 2006

INVENTOR(S) : William D. Llewellyn

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Claims:

In line 7 of claim 20 (column 10, line 15) change "byte" to --by the--.

MAILING ADDRESS OF SENDER:

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PATENT NO. 7,026,866 B2

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